United States Patent

[11] 3,579,030

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[73] Assignee The Strand Electric & Engineering Company Limited London, England
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[33] Great Britain
[31] 20,462/67

[54] **STAGE LIGHTING CONTROL UNIT**
12 Claims, 4 Drawing Figs.

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[51] Int. Cl. H05b 37/00
[50] Field of Search 315/291, 292, 293, 307, 312, 313, 314, 315, 316, 317, 320, 321, 294, 295

[56] **References Cited**

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3,004,193 10/1961 Bentham et al. 315/316X
3,221,214 11/1965 Wolff et al. 315/292
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Primary Examiner—John W. Huckert
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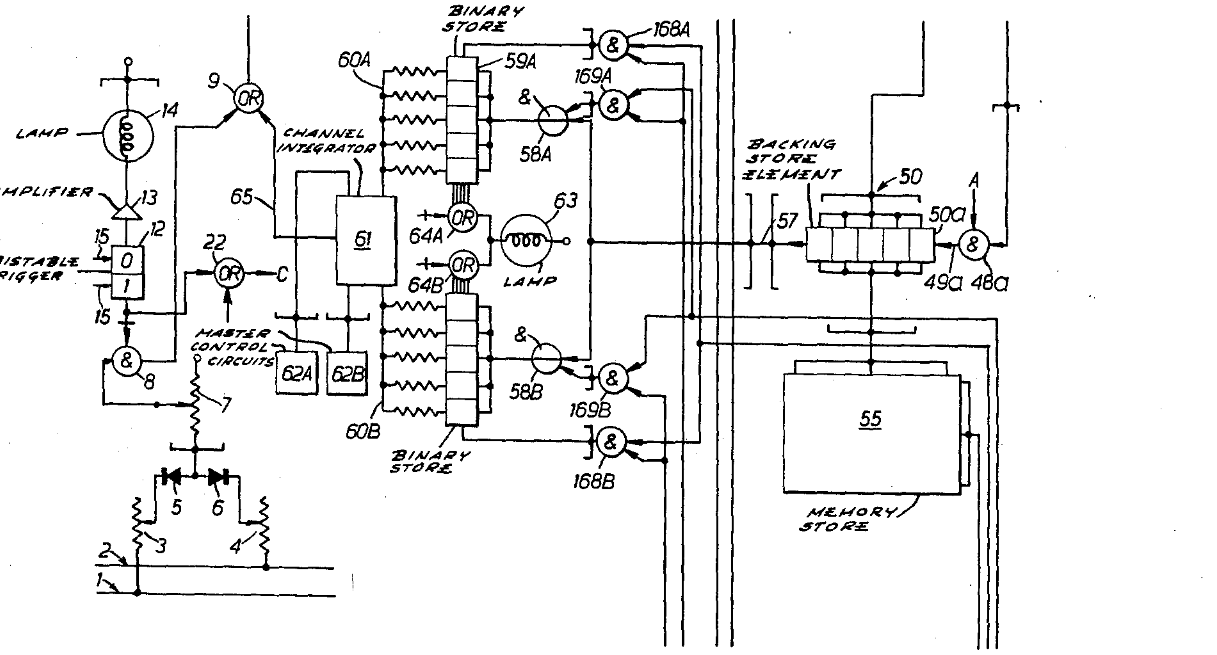
ABSTRACT: A stage lighting control unit in which dimmer line signals are recorded in a memory unit for subsequent recall, and in which an active memory connected between the dimmer lines and the memory store includes a backing store for reading information into and out of the memory unit and also includes a pair of individual active memory elements into which information can be written from the backing store for transmission to the dimmer lines.



Patented May 18, 1971 3,579,030

4 Sheets-Sheet 1

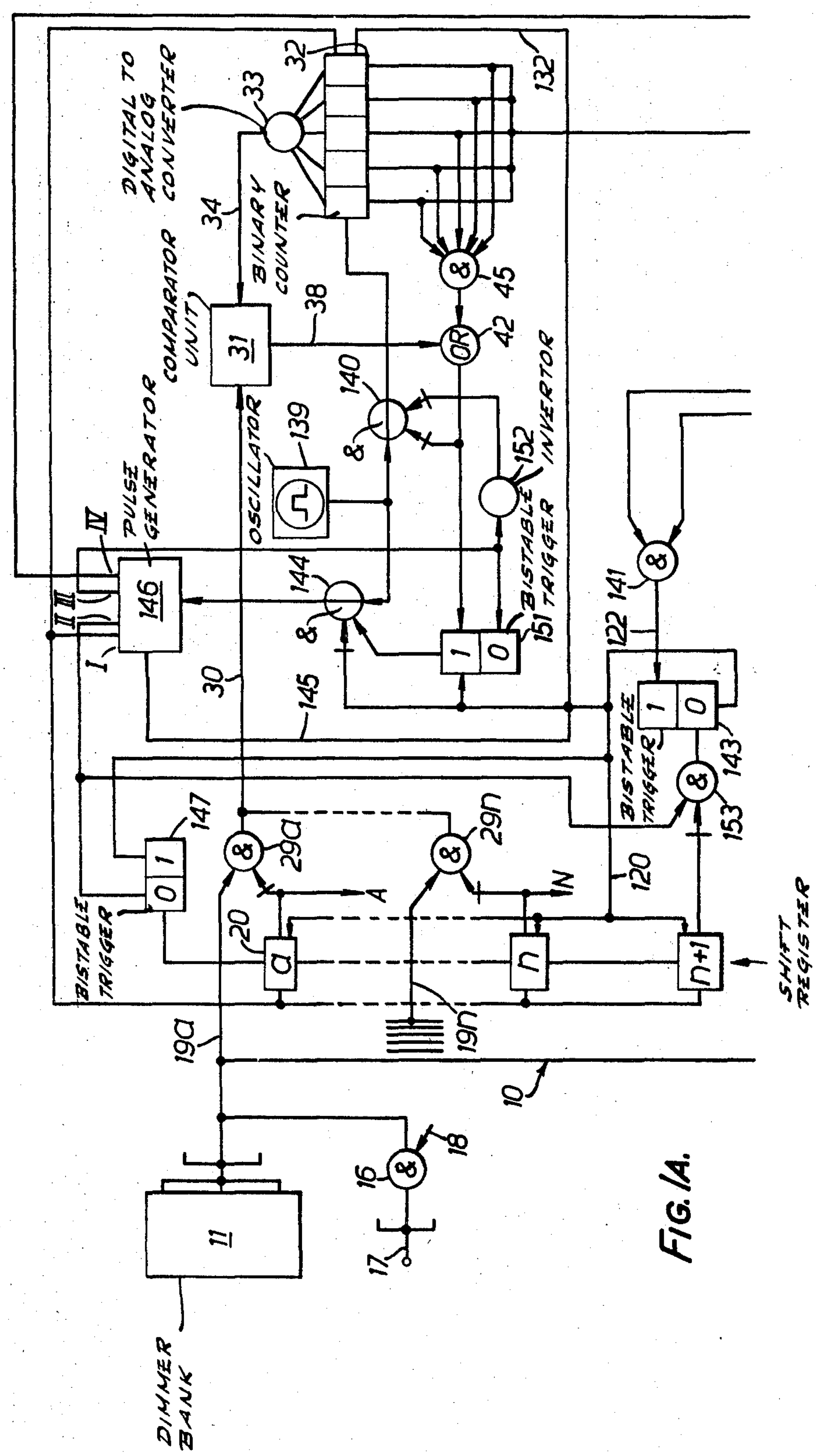


FIG. 1A.

Patented May 18, 1971

3,579,030

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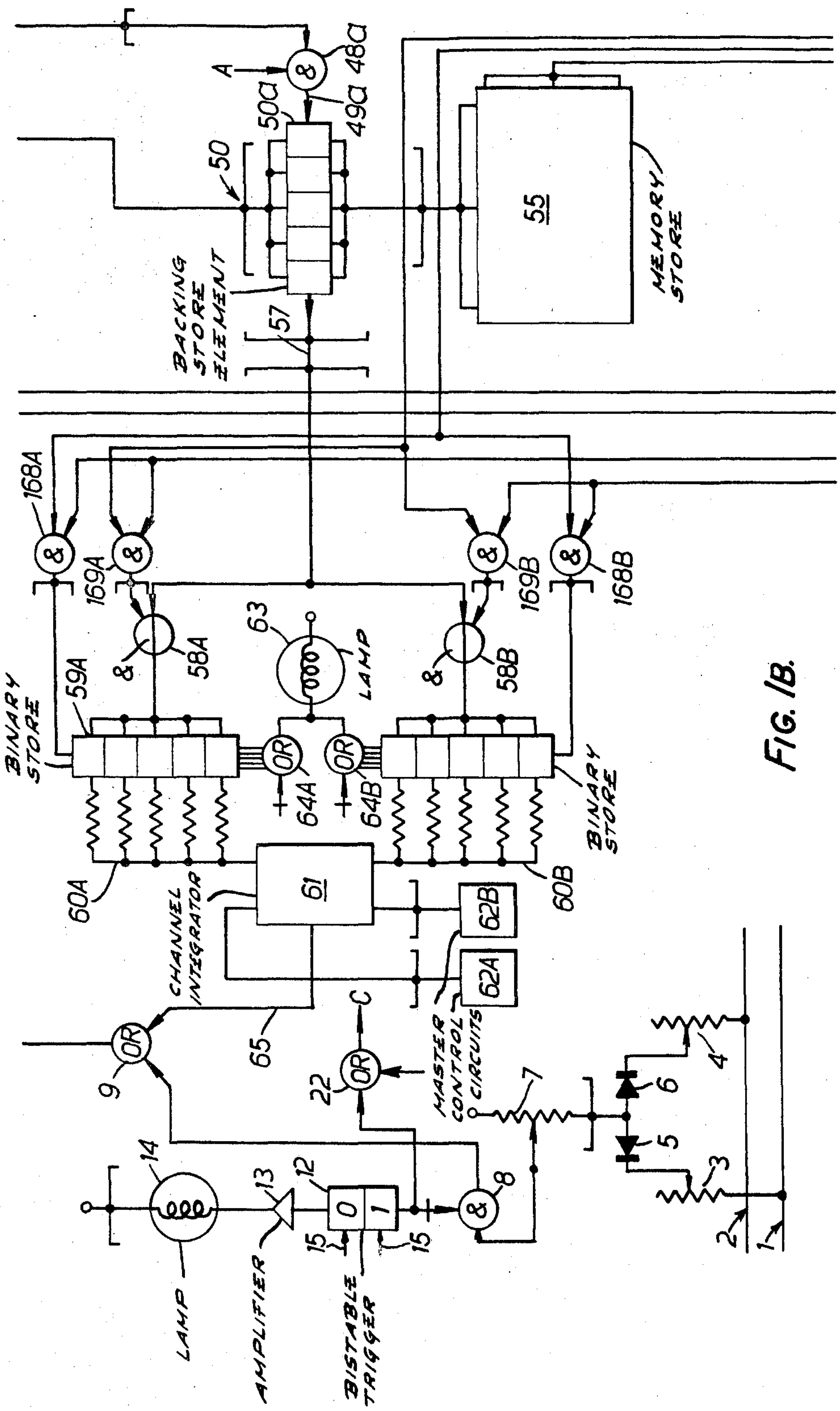

FIG. 1B.

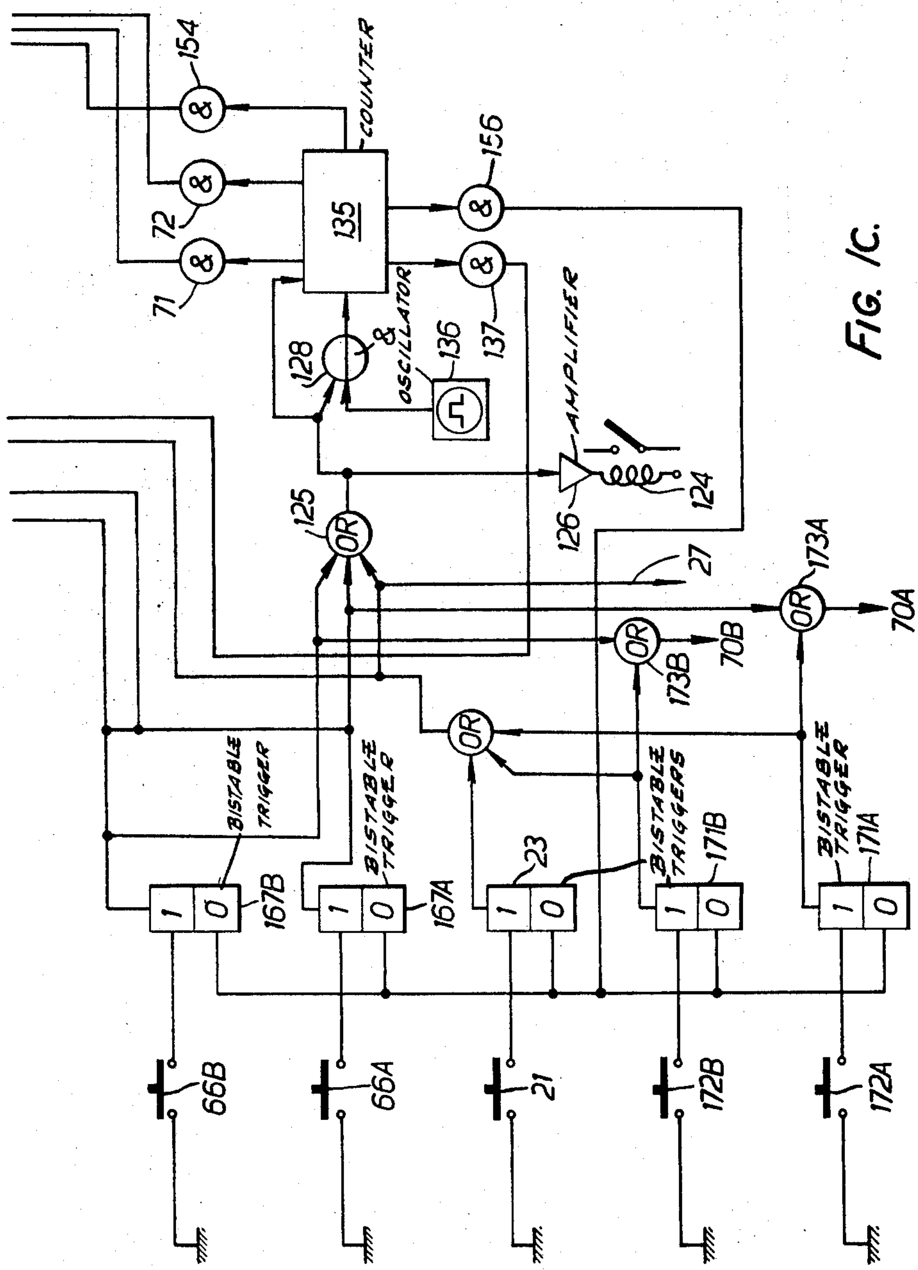
154
COUNTER
72
71
135
156
137
128
&
OSCILLATOR
136
AMPLIFIER
126
124
125
OR
27
173A
70A
173B
70B
BISTABLE TRIGGER
167B
BISTABLE TRIGGER
167A
23
BISTABLE TRIGGERS
171B
BISTABLE TRIGGER
171A
66B
66A
21
172B
172A

FIG. 1C.

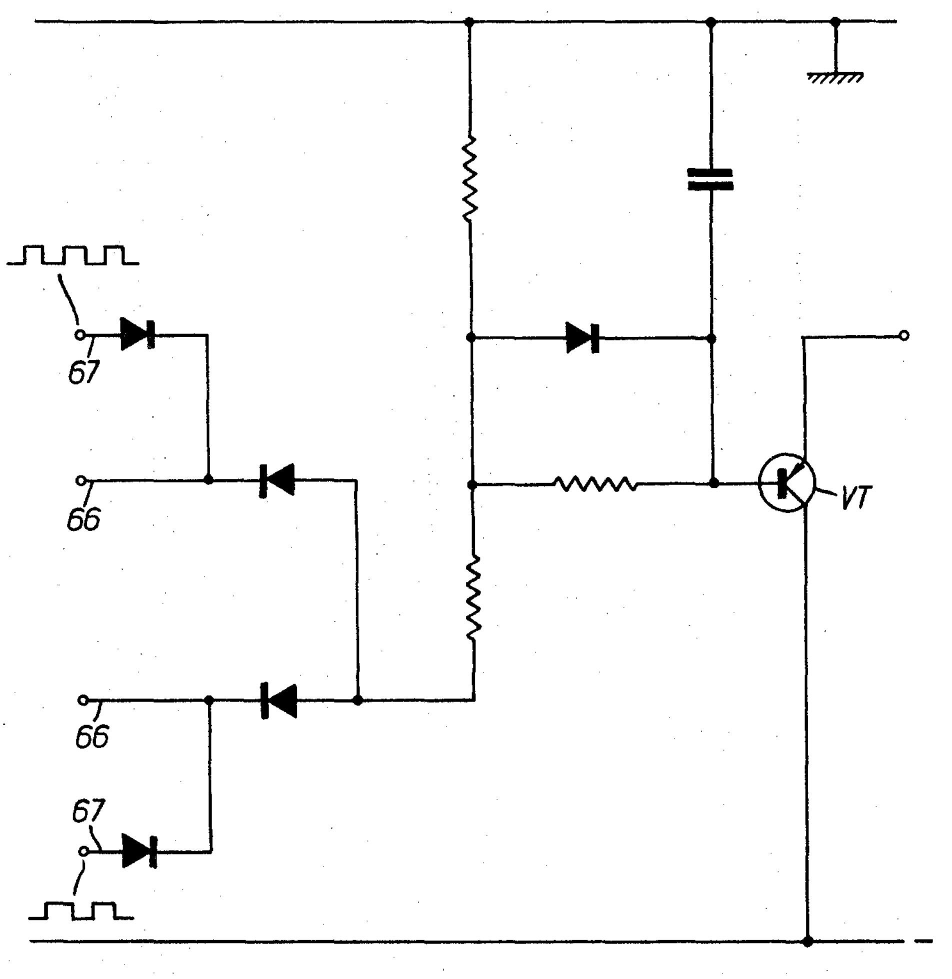

FIG. 2.

STAGE LIGHTING CONTROL UNIT

This invention relates to stage lighting control units and is an improvement of the invention described and claimed in U.S. Pat. No. 3,448,338. Claim 1 of that patent claims "A stage lighting control unit comprising in combination:

a. a memory store having "write" and "read" lines and defining a plurality of lighting effect memory elements and a continuously modifiable "active" memory element,

b. a dimmer control signal generator having an output which is connectable to the "write" line corresponding to said "active" memory element, said generator, when said output is so connected, operating continuously to modify the contents of the "active" element thereby defining a sequence of dimmer control signals in said "active" memory element for storage in a corresponding lighting effect memory element from said plurality thereof,

c. a master fader unit having an input that receives the concurrent value of a sequence of dimmer control signals from the "read" line of said "active" memory element,

d. a plurality of dimmers having corresponding inputs connected to said output of said master fader whereby each of said dimmers is controlled in dependence upon the concurrent value of the corresponding dimmer control signal in the sequence in said "active" memory element subject to continuously variable control by the dimmer control signal generator, and

e. display means associated with each of said dimmers and having an input connected to a second output of said master fader thereby to indicate the application of control signals to each of said dimmers."

Claim 2 of said U.S. patent claims "A stage lighting control unit as claimed in claim 1 in which are provided two continuously modifiable "active" memory elements, said two "active" memory elements being alternatively connectable to said lighting effect memory elements, said output of said dimmer control signal generator also being alternatively connectable to either of said two "active" memory elements and said input of said master fader unit being connected to the "read" line of the "active" memory element of which said output of said dimmer control signal generator is connected at any time." The present invention is an improvement of the system claimed in claim 2 of U.S. Pat. No. 3,448,338, wherein there is provided in the "active" memory element, in addition to said two continuously modifiable memory element a backing store having lines connected in information-transmitting relationship to and from said lighting effect memory elements, and a further set of lines connected to said continuously modifiable "active" memory elements whereby information passes solely from said backing store into said continuously modifiable "active" memory elements.

Conveniently, information transmitted to the memory store is derived from the dimmer lines and fed to the backing store.

The invention will now be described in greater detail with reference to the accompanying drawings, of which:

FIG. 1 is a schematic representation of the circuit of one embodiment of the invention; and

FIG. 2 is a detail of the active memory portion of FIG. 1.

The dimmer control signals in the illustrated embodiment are derived from lines 1 and 2, which are connected via corresponding master potentiometers 3 and 4 and isolating diodes 5 and 6 to a plurality of dimmer control potentiometers, one of which is illustrated at 7. The output from each dimmer control potentiometer passes via a corresponding AND gate 8 to one input of a two-input OR gate 9 whose output passes along a line 10 to the corresponding channel of a dimmer bank 11. Control of the gate 8 is effected by means of a corresponding bistable trigger 12, one side of which applies inhibiting signals to the gate 8 and the other side of which acts via an amplifier 13 to energize a red signal lamp 14 located within the scale of the potentiometer 7. Triggering of 12 is effected via lines 15 which may be energized either by individual channel switches or by master switches. The side of bistable trigger 12 connected to the gate 8 is also provided with an output C which is used to cancel the corresponding active memory elements via OR gate 22. The active memory element may also be cancelled by individual switches via OR gate 22. Each dimmer line 10 is further connected, via a gate 16, to a common line 17 leading to a dimmer level meter which is not shown in the drawings. The other input 18 to gate 16 is taken from a microswitch in the channel dimmer control 7, so that when the scale of the control 7 is depressed, the actual dimmer signal on the corresponding line 10 is displayed on the level meter.

Each of the n dimmer lines 10 has connected to it a further line 19a—19n. Each of these lines 19 is associated with a corresponding stage of a shift register 20 which is in fact a shift register of (n+1) stages, the (n+1)th stage of the register being used purely for switching purposes. The shift register is such that during operation all stages contain one bit of information, and a 0 is stepped from stage to stage in response to shift pulses. Each stage of the shift register has an output connected to inhibit input of a corresponding AND gate 29, and the corresponding line 19 is connected to the other input of this gate. Thus, as shown in FIG. 1, stage 20a of the shift register is connected to the inhibit input of gate 29a, the other input of which is connected to line 19a. The outputs of all the gates 29 are connected to a common line 30, which is connected to one input of a comparator unit 31. The signal on the line 30 at any time can be compared by the comparator with the existing count in a five-stage binary counter 32. A digital-to-analogue converter 33 converts the count in the counter to a corresponding analogue signal, and this is passed on a line 34 to the second input of the comparator 31. The counter 32 is stepped by an oscillator 139 which produces a 50 kc./s., square wave. The output of the oscillator is connected to two AND gates 140 and 144, the output from gate 140 is connected to the counter 32, while the output from gate 144 is connected to the input of a pulse generator 146. The pulse generator 146 takes the form of a cyclically connected shift register which has four outputs, I, II, III and IV, pulses appearing successively at these outputs in response to pulses from the oscillator 139.

Operation of the shift register 20 and successive circuitry described above is initiated by a signal on a line 122 which sets bistable trigger device 143. In its reset condition, the trigger 143 has served to maintain the shift register 20 reset via a line 120, to maintain counter 32 in a reset condition over a line 132, to maintain pulse generator 146 in a reset condition over line 145, to maintain in its set condition a bistable trigger device 147 while 0 state is connected to the first stage of the shift register 20, and also to maintain in its set condition a further bistable trigger device 151, whose output would normally unblock gate 144 to oscillator pulses, but which is overridden by a direct inhibit input to gate 144 from the 0 side of bistable trigger device 143. When the pulse on line 122 sets trigger device 143, the shift register 20, counter 32, bistable trigger devices 147 and 151 remain in their existing conditions, but as the inhibit input from bistable trigger device 143 is removed from gate 144, pulses from oscillator 139 can now pass via gate 144 to pulse generator 146, which produces a first pulse at its output I. This pulse serves two purposes. Firstly, it sets the counter 32 to register binary number 11111 representing "full light", and secondly, it applies a shift pulse to the shift register thus writing 0 into stage 20a. Thus, the inhibit signal is removed from gate 29a and line 19a is connected to line 30. The remaining stages of shift register 20 all contain one bit of information, and so the remaining gates 29 are inhibited. Thus, only the dimmer signal on line 10a appears on line 30. During this process the gate 140 has remained blocked. On receipt of the next pulse from oscillator 139, pulse generator 146 produces an output on its terminal II. This resets bistable trigger device 147 and is also fed to one input of an AND gate 153 whose output is connected to reset bistable trigger device 143. However, the second input to gate 153 carries an inhibit signal at this stage, and so device 143 remains set. The third pulse from pulse generator 146 emerges from output III. This pulse resets bistable trigger device 151, and is inverted by an invertor circuit 152 to remove the inhibit at one input of gate 140, thus unblocking this gate to permit oscillator pulses to pass to counter 32. Meanwhile, the resetting of bistable trigger device 151 has resulted in blocking of gate 144 so that no further pulses will pass from oscillator 139 to pulse generator 146.

The pulses reaching counter 32 from AND gate 140 serve to decrease the count in the counter in decrements of one binary digit. This decrease of count continues until the signal on line 34 falls below the signal on line 30, upon which the comparator 31 will produce an output signal on line 38, the output signal passing via the OR gate 42 to apply an inhibiting input to gate 140, thus immobilizing the counter, and also to set bistable trigger device 151 again, thereby unblocking gate 144 in the absence of the inhibit from bistable trigger device which is still set. The next pulse from oscillator 139 passes to pulse generator 146 and an output pulse appears at output IV of the latter. This pulse passes via an AND gate 48*a*, the other input of which carries a signal A from the output of state 20*a* of the shift register, and instructs the backing store element 50*a* to copy the count in the counter 32. Since this count corresponds to the signal on the line 19*a* this signal has effectively been recorded in the backing store element 50*a*.

With the gate 144 unblocked, the oscillator continues to supply pulses to pulse generator 146. The pulse from output I applies a shift pulse to the shift register, and the 0 condition is stepped into stage 20*b* of the register. Simultaneously, the count in counter 32 is set to the "full light" condition. The pulse from output II of the generator 146 is redundant, since during this cycle of operation the bistable trigger device 147 is already reset. Again, the pulse applied from output II to the AND gate 153 is also ineffective, since there is an inhibit output from the (*n*+1)th stage of the shift register. The effect of the third and fourth pulses is identical to that described in relation to the first cycle of operation and it will be readily understood that the effect of the presently described cycle is to write into counter 32, and thence to backing store 50*b*, a binary number corresponding to the signal on dimmer line 10*a*. This process continues until all the backing stores 50 contain information corresponding to the signals on the respective dimmer lines 10. When the last backing store, 50*n*, has been filled, the next pulse from output I of the pulse generator 146 causes the 0 condition to be passed into the (*n*+1)th stage of the shift register. Then, the output on II causes AND gate 153 to reset bistable trigger device 143 thereby terminating the recording process, and switching the shift register, counter 32, pulse generator 146 and bistable trigger devices 147 and 151 to their rest states in readiness for a further recording operation.

The contents of the backing stores 50 may then be stored in a memory store 55 for later use. Alternatively, if a lighting effect is being built up on stage, or in the event of failure of the memory 55, information recorded in the backing stores 50 can be used directly to control the dimmers in the bank 11. Assuming the backing stores to contain a complete set of information, this is utilized by transferring the contents of the stores on lines 57, via parallel connected AND gates 58A and 58B to a corresponding pair of binary stores 59A and 59B respectively. The outputs of the stores 59A and 59B are fed via resistive digital-to-analogue converters indicated to 60A and 60B to the inputs of a channel integrator 61. Master control circuits 62A and 62B control the channel integrator so that in normal operation the output of the channel integrator is fed by that A or B store 59 whose master control is set higher. The actual output is the analogue value stored in the appropriate store 59, multiplied by the percentage setting of the corresponding master control circuit 62. The selection of the connection between the store 59 and the backing store 50 is governed by inputs to the gates 58A and 58B. The occupation of a selected store 59A or B is indicated by a white channel lamp 63 located in the appropriate dimmer control scale and energized via five-input OR gates 64A and 64B fed from the five stages of the corresponding store 59A or B, the gate 64 associated with the nonselected store being inhibited by a signal derived from the condition of the control circuits 62A and B. Cross-fading is also possible, in which the output of the channel integrator is proportional to the stage reached by the cross-fade, the limits of the cross-fade being the values stored in the stores 59A and 59B.

In either form of operation, the output from the channel integrator is fed on line 65 to the second input of the channel OR gate 9.

The cancelling signal C acts to cancel the contents of the stores 59A and 59B of the corresponding lighting channel. Thus, depending upon the condition of bistable trigger device 12 either the voltage at the slider of potentiometer 7 is passed via the OR gate 9 to the corresponding dimmer line 10, the contents of the stores 59A and 59B being cancelled, or alternatively the AND gate 8 is blocked and the signals in the appropriate store 59A or 59B pass on to the line 10. Thus, it will be seen that the circuit so far described enables dimmer signals on the lines 10 to be recorded in the memory 55 and subsequently to be represented on the lines 10 to control the stage lighting accordingly.

The ultimate control of the operation of the circuit is effected by a clock consisting of an oscillator 136 and a counter 135. Passage of pulses from the oscillator 136 to the counter 135 is via an AND gate 128. In its turn the AND gate is controlled by the output of an "OR" gate 125 whose five inputs are connected to bistable trigger devices 23, 167*a*, 167*b*, 171*a* and 171*b*. These trigger devices may be set in response to manual operation of a set of control switches.

Control of a recording operation is effected by means of a "Record' control switch 21, which operates to set bistable trigger device 23. Setting of the trigger device 23 generates a signal which is passed via OR gate 125 to open AND gate 128 and to reset counter 135. The output from the gate 125 also passes via an amplifier 126 to the coil 124 of a reed-relay which energizes the backing store 50. In addition to energizing the backing store and starting the counter 135 in response to the oscillator 136, the signal from bistable trigger device 23 also appears at one input of an AND gate 141 whose output is the line 122 leading to the bistable trigger device 143. Finally, the output of the trigger device 23 passes along the line 127 via a manually operable digital selector to select a given memory channel in the memory 55 into which information is to be written. An AND gate 137 detects the third and fourth states of counter 135, and during the persistence of these states the gate produces an output which appears at the second input of the gate 141. This gate 141 therefor produces an output which appears on the line 122 to initiate the recording operation referred to above. As the count on the counter 135 proceeds to the fifth state, this is detected by an AND gate 154 which produces an output which instructs the commencement of recording by the memory 55. This recording process continues until the memory is full and after this an AND gate 156 detects the 62nd, 63rd, 64th 1st and 2nd states of counter 135 to produce an output which passes, inter alia, to reset the bistable trigger device 23, thus blocking gate 128 and arresting the counter 135. The oscillator 136 produces 64 pulses per second, and this provides a clock frequency which allows adequate time for the operation of the comparator circuits to record information and pass it to the backing stores.

The recording process can now be repeated for a different combination of dimmer control signals and the contents of the backing sore 50 can then be recorded in another channel of the memory 55. In this way, a complete lighting plot consisting of as many different lighting cues as the memory contains memory channels, can be recorded for subsequent reuse.

Recall of the stored lighting cues is also controlled by the clock 136, 135. Two "Recall" switches 66A and 66B are connected to effect setting of the two bistable trigger devices 167*a* and 167*b* respectively. The "Recall A" switch 66A is associated with the binary store 59A while the "Recall B" switch 66B is associated with the binary store 59B. Each of the bistable trigger devices 167*a*, 167*b* acts in a manner similar to bistable trigger device 23 to reset and initiate counting in the counter 135, also energizing the backing stores 50. However, instead of acting on the comparative circuitry, the outputs from these two trigger devices pass to corresponding AND gates controlling the binary stores 59A and 59B.

Assuming that switch 66A has been operated, then simultaneously with the starting of the clock circuit, signals are applied to a pair of AND gates 168*a* and 169*a*. As the counter 135 reaches its fifth state, the memory 55 is instructed via AND gate 154 to write into the backing stores 50 the information contained in a channel selected by a digital selector energized via line 70*a*. Backing stores 50 have already been energized for this operation via amplifier 126.

The output of gate 168*a* is connected to cancel the contents of binary store 59A, and this function is exercised when a signal is applied to the second input of the gate by an AND gate 71 which recognizes the 60th state of counter 135. The output from gate 71 also applies a signal to a corresponding input of an AND gate 168*b* corresponding to binary store 59B, but as there is no output from the bistable trigger 167*b* corresponding to "Recall B" switch 66B, gate 168*b* does not produce an output. When the counter 135 reaches its 61st state, this is recognized by an AND gate 72, and a pulse is passed to a second input of the AND gate 169*a*, whose output then acts to unblock AND gate 58*a* to write the contents of the backing store 50A into the binary store 59A. The contents of the binary store 59 can then be used as described above to control the stage lighting. The output from AND gate 72 is also passed to the gate 169*b*, but again, since there is no output from bistable trigger 167*b*, this gate also remains blocked.

In this way, information in each of all the backing stores 50 is simultaneously written into the corresponding binary stores 59A for subsequent use. It will be appreciated that corresponding entry of information into binary stores 59B is effected in a similar manner by means of the "Recall B" switch 66B. It is possible to record in store 59B while store 59A is in use, and in this way cross-fading between two lighting effects can be carried out by means of the control circuits 62A and B. Should the memory 55 fail for any reason, then it is possible to continue to use the equipment on the basis of two preset channels by writing each lighting effect into the backing store 50 and passing it alternately to the binary stores 59A and 59B. Whichever mode of operation is employed, the bistable triggers 167*a* and 167*b* are reset by the output of the AND gate 156 at the completion of the operation, in a manner similar to that described in relation to the resetting of bistable trigger device 23.

If it is required to modify a recorded effect, then the "Rerecord" switches 172A and 172B are used. Assuming that the effect which is to be modified is contained in the binary store 59A, then procedure is as follows. Firstly, the level of illumination given by the particular channel to be modified is read out from the line 17 by depressing the scale of the appropriate control 7. The lever 7 is then moved to a position corresponding to the reading of the meter, and an individual channel selector is pressed to set the bistable trigger device 12, thus opening the AND gate 8 and applying an inhibiting signal C to the corresponding section of binary store 59A. This results in the resumption of control of the particular dimmer by the potentiometer 7 without change in intensity of the lamp. The effect that the potentiometer 7 now controls the channel is indicated by the extinguishing of the corresponding white lamp 63 in the potentiometer scale, and the illumination of the red lamp 14. The potentiometer 7 is then adjusted until the desired lighting is provided by the corresponding lamp, and the "Rerecord A" switch 172A is operated. This causes bistable trigger 171*a* to set, thus passing a signal via OR gate 125 to carry out the necessary starting of the counter 135 and energizing of the backing stores 50. In addition, the output of the bistable trigger 171*a* is passed to gate 14 to set in motion the operation of the comparator circuit as if for a normal recording operation. However, to ensure that the modified lighting effect is recorded in the same section of memory 55 that is occupied by that effect previous to modification, the selection of the correct memory channel of memory 55 is effected via an OR gate 173*a* on line 70*a* which was previously energized for the recording of the effect undergoing modification. This not only saves the provision of a pair of further digital selectors, but also simplifies the operation of the unit. Upon the completion of the rerecording operation, the trigger device 171*a* is reset by the output from AND gate 156. Rerecording of a lighting effect contained in binary store 59B is effected in a similar manner by means of "Rerecord B" switch 172B.

A typical operation involving the illustrated channel control potentiometer will now be described. In order to select the channel, an "individual transfer" switch is operated, to drive the bistable trigger 12 into its 0 state. This has three effects, namely to illuminate the red lamp 14 within the potentiometer scale, to remove the inhibiting input from gate 8 and to cancel the stores 59A and 59B. Thus, the only signal to appear at the output of OR gate 9 is that determined by the potentiometer 7 and whichever of the potentiometers 3 and 4 is operative. This signal controls the channel dimmer in the bank 11, and the stage light assumes the appropriate intensity. The channel may be deselected at any time by pressing a "trip" switch, the effect of which is to drive the trigger 12 to its 1 state, inhibiting the gate 8 and switching off the red lamp 14. In this way, a lighting effect may be built up, with the position of the potentiometer levers indicating the levels in the channels, and the red lamps indicating which channels are selected. Recording of the light effect is then carried out by actuating the switch 21, as described above. At this stage the lamps are still under the direct control of the potentiometers 3, 4 and 7. If it is wished to modify the same effect, this is done by operating the appropriate channel controls and rerecording the effect in the same section of the memory 55. It is possible to select all the dimmer channels by actuating a "master transfer" switch which has the effect of driving all the bistable triggers 12 to their 0 state.

To retrieve a recorded effect, a "master trip" switch is actuated to deselect all channel potentiometers, the numerical selector is set to select a desired section of the memory, and one of the sets of gates 58 is opened. Information is then written into the backing stores 50 and transferred to the relevant A or B stores 59, and the white lamp 63 in the scale of the potentiometer of each channel containing recorded information is illuminated. The digital output from each A and B store is then converted to analogue form, passed to the integrator 61, where it is modified by a constant factor determined by the setting of the master control 62, and thence, via the OR gate 9 to the dimmers.

It is also possible as described above, to modify the on-stage lighting produced by a recorded effect. To do this, in practice, the potentiometer scale of the appropriate channel is depressed to discover the prevailing level in that channel. The dimmer lever is then moved to the corresponding valve, when the "individual transfer" switch is depressed. As previously describe, this causes cancellation of the corresponding store 59, but since the dimmer potentiometer 7 has the same setting as the recorded level, no interruption of stage light occurs. The selected channel is now under the control of its potentiometer, the red potentiometer scale lamp is illuminated to distinguish the fact, and the light on stage may be modified by adjustment of the channel potentiometer. The change is not instantaneously recorded, but circuits are provided to illuminate a warning lamp in the switch button 21 as soon as a "-transfer" switch is actuated during playback, thus giving a warning that unrecorded changes may be present on stage. Pressing the "Record" switch 21 will cause rerecording of the effect, and any alterations will also be recorded. At this stage, the potentiometers of "transferred" channels will show both red and white lamps, since the previously cancelled stores 59 will, if not amended to zero light, be refilled to open the corresponding OR gates 64. These channels may then be "tripped", causing extinction of the red lamps, and resumption of control by the memory, or alternatively they may be left "-transferred" to cause analogous alteration of subsequent recorded effects.

When performing a recorded lighting plot, it will be normal to use the A and B stores 59 alternately, since cross-fading can then be carried out by the use of the master controls 62. The memory store 55 of the illustrated embodiment has 256 channels, which is normally adequate to cater for each lighting change in a lighting plot, but extra, unrecorded, effects can be produced by using, in addition to the A and B mastered stores 59, groups of lights controlled directly from the potentiometers 7, which may be further grouped onto the master potentiometers 3 and 4.

It will be seen from the above description that the backing stores 50, together with the A and B stores 59, constitute the portions of an active memory, via which all writing and reading of information in the memory store 55 takes place. Further, the white lamps 63 are provided so that during playback, when the levers of the potentiometers 7 do not represent the state of lighting on stage, the application of a dimmer signal to each lighting circuit for a given lighting effect is presented visually in response to the dimmer control signals in the memory section containing the lighting effect.

Mastering and cross-fading of the contents of the A and B stores 59 is carried out in the present embodiment by means of square wave trains from the master control units 62A and B. FIG. 2 represents the integrator 61 of a lighting channel, and it will be seen that the output response of transistor VT is controlled by the signals on the leads 66, which are connected to resistance networks 60, and 67, which are fed with the square wave trains from master units 62. Normal mastering is carried out by varying the mark/space ratio of the square waves, the leading edges of which are in phase in this application. The output from the transistor passes onto a common line, and the "higher" (i.e., longer) master signal controls the relevant dimmer.

During normal operation, as stated, the leading edges of the two trains of square waves fed to the integrator are in phase, but for cross-fading they are arranged to be in antiphase, so that continuous change of mark/space ratio causes one channel signal to fade as the other increases, the output being equal to the sum of the signals on leads 66, but never more than the maximum output of resistance network 60.

It is found in use that the circuit of FIG. 2 enables a "-dipless" cross-fade to be produced. This results from the simultaneous smoothing of both square waves by the capacitor C1, which provides a smoothly varying average value as the cross-fade proceeds.

We claim:

1. An improved stage lighting control unit of the kind comprising in combination:

a. a memory store having "write" and "read" lines and defining a plurality of lighting effect memory elements and two continuously modifiable "active" memory elements, said two "active" memory elements being alternatively connectable to said lighting effect memory elements,

b. a dimmer control signal generator having an output which is connectable to the "write" line corresponding to either of said "active" memory elements, said generator, when said output is so connected, operating continuously to modify the contents of the "active" memory element thereby defining a sequence of dimmer control signals in said corresponding "active" memory element for storage in a corresponding lighting effect memory element from said plurality thereof,

c. a master fader unit having an output that receives the concurrent value of a sequence of dimmer control signals from the "read" line of one of said "active" memory elements, and an input connected to the "read" line of the "active" memory element to which said output of said dimmer control signal generator is connected at any time,

d. a plurality of dimmers having corresponding inputs connected to said output of said master fader whereby each of said dimmers is controlled in dependence upon the concurrent value of the corresponding dimmer control signal in the sequence in said corresponding "active" memory element subject to continuously variable control by the dimmer control signal generator, and

e. display means associated with each of said dimmers and having an input connected to a second output of said master fader thereby to indicate the application of control signals to each of said dimmers,

wherein the improvement comprises the provision in the "active" memory element, in addition to said two continuously modifiable memory elements, of a backing store having lines connected in information-transmitting relationship to and from said lighting effect memory elements, and a further set of lines connected to said continuously modifiable "active" memory elements whereby information passes solely from said backing store into said continuously modifiable "active" memory elements.

2. A stage lighting control unit as claimed in claim 1 wherein said dimmer control signal generator has an input circuit connected to said dimmer input lines.

3. A stage lighting control unit as claimed in claim 2 in which said "active" memory elements have outputs connected to said inputs of said dimmers via OR gates located ahead of said input circuit of said dimmer control signal generator.

4. A stage lighting control unit as claimed in claim 3 in which said dimmer control signal generator input circuit includes a selector having inputs connected to said dimmer input lines and a single output connected to said dimmer control signal generator.

5. A stage lighting control unit as claimed in claim 4 in which said selector is a shift register.

6. A stage lighting control unit as claimed in claim 5 in which said output of said output of said selector is connected to one input of a comparator having a second input fed from a signal generator which itself has an output connected to said backing store, said comparator having an output connected to a control terminal of said signal generator thereby controlling the output of said signal generator in accordance with the signal on said selector output.

7. A stage lighting control unit as claimed in claim 6 wherein said signal generator is a binary counter connected via a digital-to-analogure converter to said second input of said comparator.

8. A stage lighting control unit as claimed in claim 7 wherein an oscillator is provided having an output connected both to a stepping input of said binary counter and also to an input of a pulse generator having outputs controlling said shift register, said binary counter, and said oscillator, the output of the latter being gated by output signals from said comparator.

9. A stage lighting control unit as claimed in claim 8 wherein there is provided a clock pulse generator having outputs connected to controlling terminals of said memory store and said "active" memory elements.

10. A stage lighting control unit as claimed in claim 1 wherein both individual "active" memory elements have outputs connected to the inputs of a binary integrator, the latter having control terminals connected to the outputs of master control circuits.

11. A stage lighting control unit as claimed in claim 10 wherein said master fader includes first and second control and signal input terminals respectively corresponding to said two individual "active" memory elements, said control input terminals being connected to the outputs of two corresponding square wave generators, and all said input terminals being connected in parallel to an input of a smooth circuit having an output connected to an appropriate dimmer line.

12. A stage lighting control unit as claimed in claim 11 wherein said two square wave generators operate in antiphase with a variable mark/space ratio.